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DESIGN OF REED SOLOMON FORWARD ERROR CORRECTION (RSFEC) AND DEVELOPMENT OF VERIFICATION MODEL

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Original research

A B S T R A C T

Reed Solomon belongs to the family of Bose-Chaudhuri-Hocquenghem (BCH) codes, but is distinguished by having multi-bit symbols. This makes the code particularly good at dealing with bursts of errors because, although a symbol may have all its bits in error, this counts as only one symbol error in terms of the correction capacity of the code. The reliability of data transmission is a constant concern, especially in applications where errors can have severe consequences. Companies developing communication components, such as HDMI, DisplayPort, or USB, face the challenge of ensuring the correctness of their RSFEC implementations. The absence of a standardized verification model complicates the validation process, leading to potential errors in communication systems. Here using Questa Sim a generic verification model is build which ensures the correctness of RS codes.

1. INTRODUCTION

Error corrections codes are used so as to maintain the data reliability (Clark & Cain, 2013; Clemente et al., 2022). During transmission of data through wireless channels like USB or HDMI with very high data rate (Sherratt & Cadenas, 2010) will give rise to error, therefore in order to detect and correct the error during the time of transmission is necessary so that receiver end gets corrected data within time (Ehlert, 2005). Reed Solomon (Figure 1) is linear, non-binary cyclic code operates over q elements of the Galois field GF(q), with q>2 (Solomon, 1993; Wicker & Bhargava, 1999).

RS (n, k) able to correct any error pattern of size t or less is defined over the Galois field GF (q^m), with parameters as:

Length of codeword	$n=q^m-1$
Number of parity bits	$n-k=2t$
minimum distance	$d_{\min} = n-k + 1$

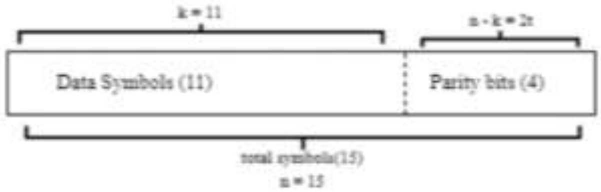

Figure 1. Reed Solomon Codeword

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RS codes are made up with m-bit symbols, and are written in the form given below:

$$(n, k) = (2^m - 1, 2^m - 1 \pm 2t)$$

Where k is the number of data symbols or information symbols, and n is the total number of code symbols in the block, t is the error correcting capability of the code, m is the size of symbol and 2t is the number of parity symbols or redundant symbols.

2. METHODOLOGY

2.1 Galois field

A Galois field consists of a set of elements (numbers). The elements are based on a primitive element, usually denoted α, and take the values:

$0,\ \alpha^0, \alpha^1, \alpha^2, ..., \alpha^{N-1}$

to form a set of 2^m elements, where $N=2^m - 1$. The field is then known as $GF(2^m)$.

The value of a is usually chosen to be 2, although other values can be used. Having chosen α, higher powers can then be obtained by multiplying by α at each step.

2.2 Primitive polynomial

An important part of the definition of a finite field, and therefore of a Reed-Solomon code, is the field generator polynomial or primitive polynomial, p(x) (Wicker & Bhargava 1994, Lin, Chung & Han 2014). This is a polynomial of degree m which is irreducible, that is, a polynomial with no factors. It forms part of the process of multiplying two field elements together. For a Galois field of a particular size, there is sometimes a choice of suitable polynomials. Using a different field generator polynomial from that specified will produce incorrect results (Huczynska 2013). For this project as we are performing RS(15,11) Galois field of 2^4 will be used i.e. GF(16). For GF(16), the polynomial p(x) = x4 + x +1 is irreducible and therefore will be used in the following sections. An alternative which could have been used for GF(16) is p(x) = x4 + x3 +1.

2.3 Generator Polynomial

Generator polynomial for RS (15,11) with primitive polynomial specified for GF (16) and referring the Galois Field table for GF (2^4) for values of alpha and using those values to create g(x) which will further be used in generating parity bits.

$$\mathbf{g(x) = (x + \alpha^0) (x + \alpha^1) (x + \alpha^2) (x + \alpha^3)}$$
$$= (x + 1) (x + 2) (x + 4) (x + 8)$$
$$= (x^2+3x+2) (x+4) (x+8)$$
$$= (x^3 + 7x^2 + 14x + 8) (x + 8)$$
$$= x^4 + 15x^3 + 3x^2 + x + 12$$

This can also be expressed as:

$$g(x) = \alpha^0x^4 + \alpha^{12}x^3 + \alpha^4x^2 + \alpha^0x + \alpha^6$$

2.4 Parity generation

At each step the generator polynomial is multiplied by a factor, shown at the left-hand column, to make the most significant term the same as that of the remainder from the previous step. When subtracted (added), the most significant term disappears and a new remainder is formed. The 11 steps of the division process are as follows:

The encoded message polynomial $T(x)$ is then:

$x^{14} + 2x^{13} + 3x^{12} + 4x^{11} + 5x^{10} + 6x^9 + 7x^8 + 8x^7 + 9x^6 + 10x^5 + 11x^4 + 3x^3 + 3x^2 + 12x + 12$

or, written more simply:

1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 3, 3, 12, 12.

2.5 Syndrome calculation

We know that the T(x) is perfectly divisible by equation Therefore, in case of no errors it must evaluate to zero. When there are errors, some or all of them will result in a non-zero value and that value is called syndrome (S_i) . Where e1, e1 … ev are the locations of error and Y_1, Y_2 … Y_v are the corresponding coefficient/magnitude of the Error polynomial E(x).

2.6 Chien Search algorithm

The Chien Search algorithm is a crucial component of Reed-Solomon Forward Error Correction (RSFEC) decoding process (Ji et al., 2015). It is employed to locate the roots of the error locator polynomial, which helps identify the positions of errors within the received code word (Krachkovsky & Lee, 1997). The algorithm operates by evaluating the error locator polynomial at specific points in the Galois field (Fedorenko & Trifonov, 2002). These evaluations are then used to determine the locations of errors in the received data. The efficiency and accuracy of the Chien Search algorithm significantly contribute to the overall performance of RSFEC systems, making it a fundamental aspect of error correction in digital communication systems.

2.7 Forney's algorithm

Forney's Algorithm is another essential component of Reed-Solomon Forward Error Correction (RSFEC) decoding process (Song & Shaffer, 2002). It is utilized to determine the error magnitudes, also known as error values, corresponding to the error locations identified by the Chien Search algorithm. Forney's Algorithm computes these error magnitudes by evaluating the derivative of the error evaluator polynomial at the error locations. This process allows for the precise determination of the error values, which are crucial for correcting the errors in the received data. The accuracy and efficiency of Forney's Algorithm significantly contribute to the overall performance and reliability of RSFEC systems, making it an indispensable aspect of error correction in digital communication systems (Weisshaar et al., 2017).

3. IMPLEMENTATION AND BENEFITS

Implementation of verification model was done on Questa Sim by Mentor Graphics in System Verilog and design model for RS(15,11) was done on Xilinx Vivado 2023.2. RTL schematic was made and a simulation was created and tested by verification model itself to ensure correctness and reliability of both the models (Figure 2). Rigorous testing of verification model was done with different values and parameters to check reliability of model.

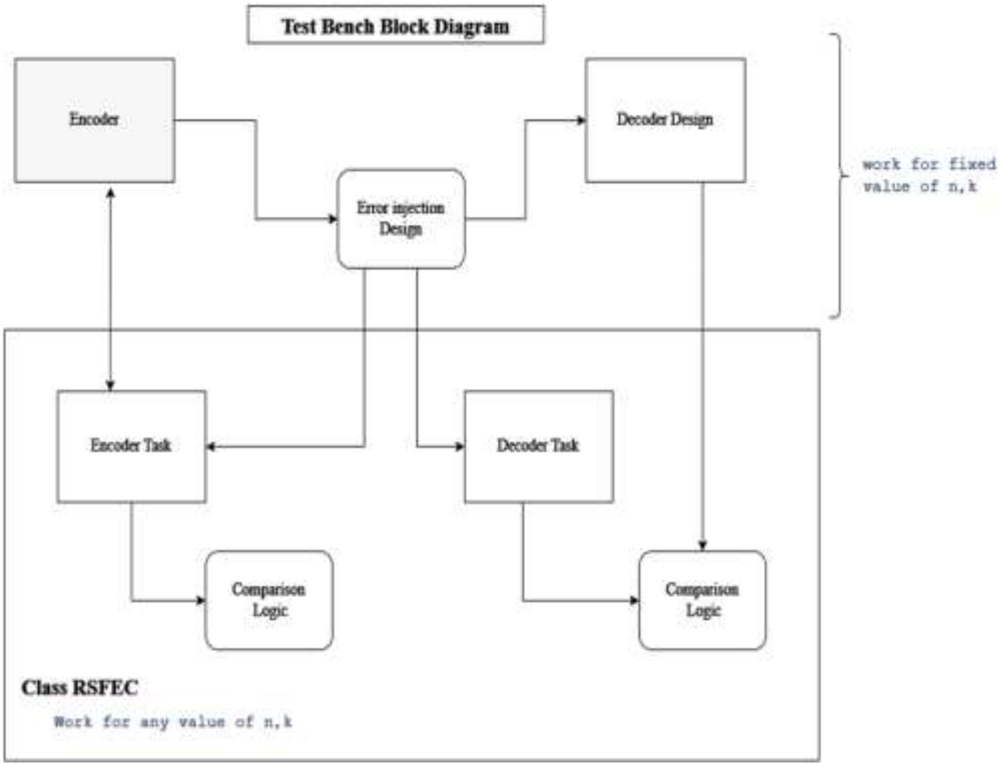
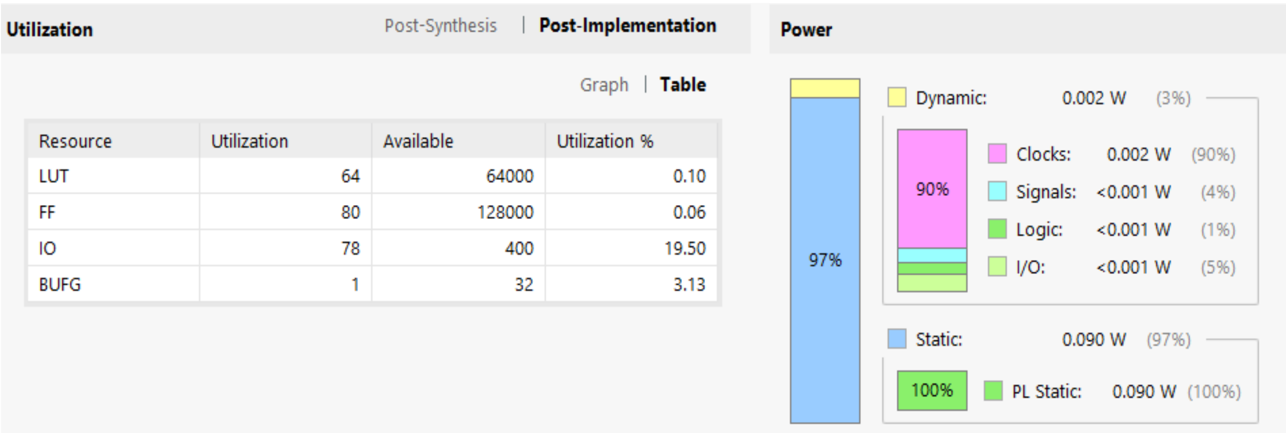


Figure 2. Block Diagram of RSFEC

3.1 Encoder Implementation

RS (15, 11) encoder implementation was done on Xilinx vivado 2023.2 on device (xc7s100fgga676-1Q) parity bits were calculated and added with message symbols and passed on from encoder. Calculation of parity bits were done dividing generator polynomial and message polynomial and xor of the terms to get the desired output.



Utilization | Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	64	64000	0.10
FF	80	128000	0.06
IO	78	400	19.50
BUFG	1	32	3.13

Figure 3. Encoder Implementation

3.2 Decoder Implementation

Decoder for RS (15, 11) was made on Xilinx vivado 2023.2 and on device xc7s100fgga676-1Q and decoding the data and checking and correcting the errors if found took numerous steps like calculating syndromes and checking if syndromes equate to 0 (for 0 errors) or the other way (Figure 3). Then using Chien search Euclidean distance and Forney's algorithm to locate the error symbol or bit and to check its magnitude and then is it correctable or not. Decoder implementation includes all these and it successfully implements all the possible situations (Figure 4).

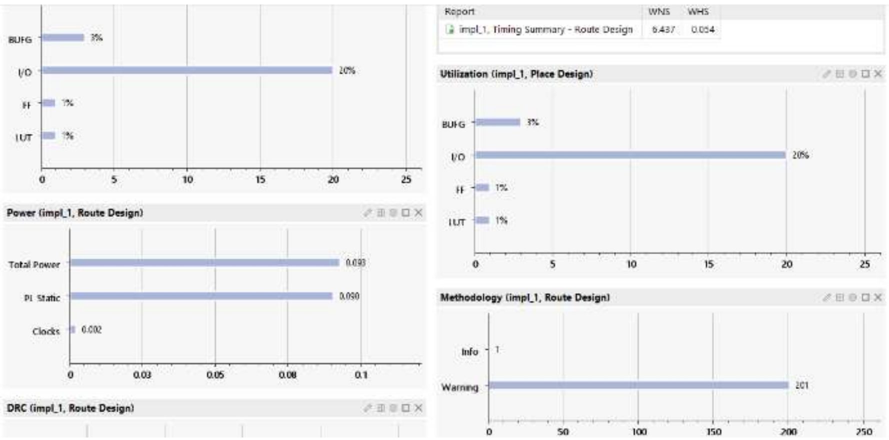


Figure 4. Statistics of implementation

Reed-Solomon Forward Error Correction (RSFEC) is a widely used error correction method in wired communication systems due to its robustness and efficiency. Here are some of the key advantages:

- Error Detection and Correction:
  RSFEC can detect and correct multiple symbol errors within a code word, enhancing the reliability of data transmission. It can correct burst errors, which are common in wired communication systems, where a sequence of erroneous bits might occur due to interference or noise.
- Improved Data Integrity:
  By correcting errors that occur during transmission, RSFEC ensures that the received data is as close to the original transmitted data as possible. This is crucial for applications requiring high data integrity, such as financial transactions, medical records, and multimedia transmissions.
- Increased Transmission Efficiency:
  RSFEC allows for higher data rates and longer transmission distances without the need for retransmission. This improves overall system efficiency and reduces latency, which is particularly beneficial in high-speed networks like Ethernet and Fiber Channel.
- Bandwidth Utilization:
  Efficient error correction means that less redundant data needs to be sent for retransmission, leading to better utilization of available bandwidth. This is particularly important in networks where bandwidth is a limited and valuable resource.
- Enhanced System Performance:
  By reducing the need for retransmissions and minimizing the impact of noise and interference, RSFEC contributes to the overall performance and stability of communication systems. It helps maintain consistent data flow and reduces the likelihood of communication breakdowns.
- Compatibility and Flexibility:
  RSFEC is compatible with various communication standards and protocols, making it a versatile choice for different types of wired communication systems. It can be implemented in both hardware and software, allowing for flexible deployment options based on the specific requirements of the system.

4. CONCLUSION

This implementation has provided a comprehensive exploration of RSFEC, an integral component of digital communication systems. Through the examination of its fundamental principles, encoding and decoding algorithms, and practical applications, we have elucidated the significance of RSFEC in ensuring the integrity and reliability of transmitted data, particularly in the face of burst errors. The development of a generic verification model using Questa Sim represents a significant contribution to the field, addressing the critical need for standardized verification methodologies in RSFEC implementations.

Moving forward, further research and development efforts can focus on refining and optimizing RSFEC algorithms and verification methodologies to meet the evolving demands of modern communication systems. Additionally, continued collaboration between academia and industry can foster innovation and drive advancements in FEC techniques, ultimately bolstering the resilience and efficiency of digital communication networks.

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